1.5v, .18u Area Efficient 32 Bit Adder using 4T XOR and Modified Manchester Carry Chain

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***Abstract*—The increasing demand for low power VLSI can be fulfilled to a great extent by making proper changes in the circuit level and architectural level design. Addition is a fundamental operation, as it is used to implement more complex functions such as subtraction, multiplication, division etc. The Manchester Carry Chain adder design is preferred to other adders, regardless the number of bits because of its high-speed and its wide applications. A new technique is presented in this paper for the implementation of a 32 bit Adder which operates at low power. Even though this implementation is structurally inherited from Manchester Carry Chain based Adder, it is highly area efficient without much increase in delay. The proposed adder is based on Multiple Output Domino logic, which helps to reduce the complexity of the adder implemented using Manchester Carry Chain adder implemented in CMOS logic. At the same time, the 4T implementations of XOR based circuits in the adder design results in lesser number of transistors for its implementation and thereby provide a low power/size solution for arithmetic functions. The simulation result shows a reduction of 23.4% in size, over CMOS adder implemented using the same Manchester Carry Chain topology at 1.5v Supply voltage with the help of TSMC .18u technology.**

***Index Terms*—Manchester Carry Chain; Low Power; Domino Pass transistor Logic; XOR; Carry Look-Ahead Adder**

I. Introduction

The demand for low power Very large Scale Integration is increasing day by day at different levels such as process technology level, architectural level, circuit and layout level. By proper selection of logic style for the implementation of functions, a considerable amount of power saving can be done in its implementation. Addition [1,4] is a fundamental operation as it is used to implement more complex functions such as subtraction, division, multiplication, etc. The advantages for carry look-ahead over other adder design are its ease of design and high speed. Among all carry look-ahead circuits, Manchester carry chain based adder circuit has the smallest transistor count. The Manchester carry chain generate the carry signals by processing signals from the carry generate and propagate blocks.

A Manchester carry chain circuit can be implemented in CMOS PTL logic, which can be used to implement different arithmetic functions. The function of the Manchester carry chain circuit is: Ck = Gk+Ck-1.Pk for k = 1 to n, where n is the bit number, Gk and Pk are the generate and propagate signals produced from two inputs of the half adder.

Domino logic gates are used to cascade CMOS dynamic gates, since dynamic gate's finite pull down time for output node to start its discharge is less. Pass transistor Logic (PTL) [4] has the advantage of being fast, and complex logic gates can be implemented with minimal number of transistors. Power consumption and circuit performance of PTL based circuits vary. However, the nMOS pass transistor does not transmit a good "1" and pMOS pass transistor cannot pass a good "0". Hence level restorers may be required at the output of logic gates.

For the implementation of sum circuits, and carry generate signals, XOR function is essential[12] and therefore the count of the transistors used for XOR implementation will reflect the size of the adder. Normal implementation of XOR function i.e. the mirror circuit implementation of XOR, in which the structure have same number of NMOS and PMOS transistors, uses 8 transistors.

PTL logic preliminaries are given in section II. The rest of the paper is as follows: Conventional Manchester Adder in section III. Then, the description of our proposed area efficient adder is given in section IV. The comparative results based on our proposed approach using Mentor Graphics ELDO Spice are given in section V.

II. Multiple Output domino Logic

The CMOS style based design is not area efficient for realization of logic function with large fan-ins[13]. So when selecting a logic style to realize a logic function, care must be taken. Pseudo NMOS technique can be used since it compromises noise margin, but static power dissipation of Pseudo NMOS technique is high. Pass transistor logic style is known to be a common method for implementing XOR based circuits, like adders. At the same time, dynamic logic style provides fast realization of logic function. But high parasitic effects is a major drawback of this logic style.

Domino Logic gates are used to cascade CMOS dynamic gates, since its pull down time for output node to start its discharge is low. Cascading similar stages at the output is done with the help of inverter at the output stage. Fig. 1 shows

the cascading of two stages in CMOS domino logic[7,8]. The operating period of a cell when its input clock and output are low is called the precharge phase. The next phase, when the clock is high, it is called evaluate phase.

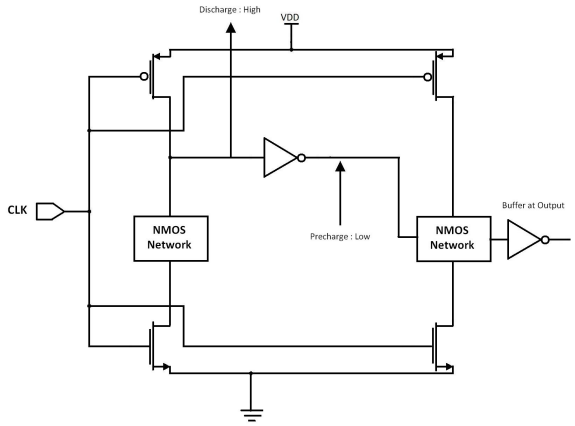

Fig. 1: Cascading of Stages in CMOS Domino Logic

When the clock is low, dynamic node is precharged to high and the output of the first buffer will become low. NMOS present in the next logic block will be in OFF condition. When the clock goes to HIGH, dynamic node is conditionally discharged and the output at the buffer will simultaneously go to HIGH state. Buffer output can only make one Low to High transition because dynamic discharge can only happen once[9].

When domino gates are cascaded and if the output of each stage rises, it will evaluate and that results in triggering the evaluation of the next stage till the last stage in the cascaded structures like a line of dominos falling[10]. Similarly, once the internal node in a gate falls, it will stay in the same state, until it is picked up by the precharge phase of the next cycle.

In Fig. 2 the PMOS keeps dynamic node at logic '1' during evaluation phase, even though it is pulled down by the NMOS network. Here the PMOS is On for all the time and hence the power dissipation will be more compared to CMOS[10].

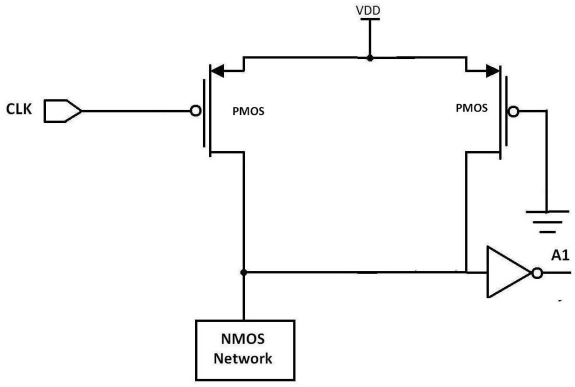

Fig. 2: Domino logic Circuit

III. Conventional Manchester adder

A carry look ahead adder is a type of adder used in digital logic. A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits compared to simple ripple carry adder[11] in which the carry bit is calculated along with the sum bit, and each bit must wait until the previous carry has been generated. This is because it need Carry_in for its correct calculation, and that was generated by the previous block. The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the next value bits.

The equation for the sum of a 4 bit Manchester carry adder will be as follows.

1) S0= A0 $\oplus$ B0 $\oplus$ Cin
2) S1= A1 $\oplus$ B1 $\oplus$ C0
3) S2= A2 $\oplus$ B2 $\oplus$ C1
4) S3= A3 $\oplus$ B3 $\oplus$ C2

The equation for the carry and carry generate and propagate of a 4 bit Manchester carry adder will be as follows.

1) Carry_out= C3
2) Ck = Gk+Ck-1.Pk for k = 1 to n
3) Gk = Ak $\oplus$ Bk
4) Pk = Ak.Bk

The circuit diagram of AND block is shown in Fig. 3. It was implemented in CMOS logic, which uses four PMOS and NMOS transistors.

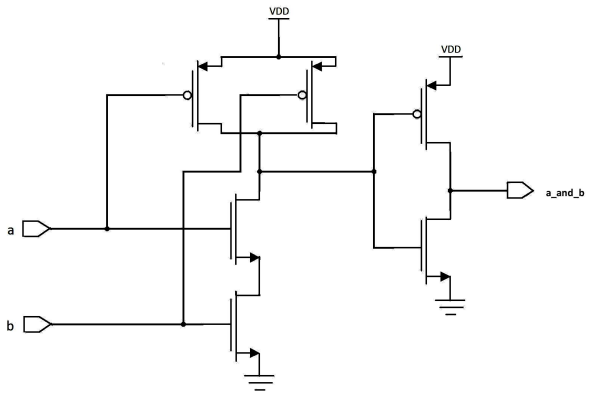

Fig. 3: AND in CMOS Logic

The circuit diagram of the Manchester carry Chain and XOR implementation of 4 bit conventional adder is shown in the Fig:4 and Fig:5. It uses a total of 27 transistors for implementing Manchester carry chain and 8 transistors for implementing the XOR function.

IV. Proposed area efficient adder

The proposed PTL quad bit adder is based on the following energy saving rules [2] and the rules are as follows.

1) The use of precharged dynamic logic, results in minimization of total charge deposited during precharge,

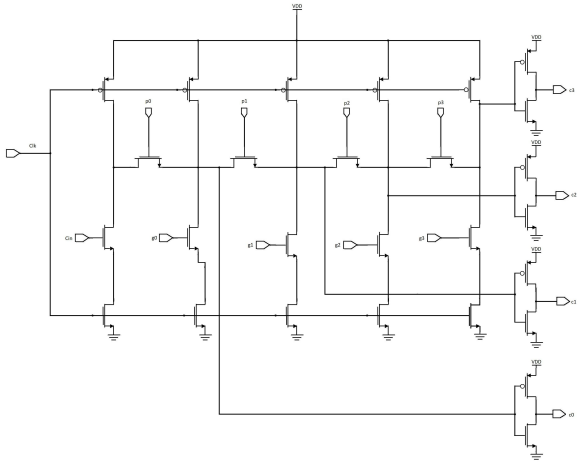

Fig. 4: Conventional Manchester Carry chain

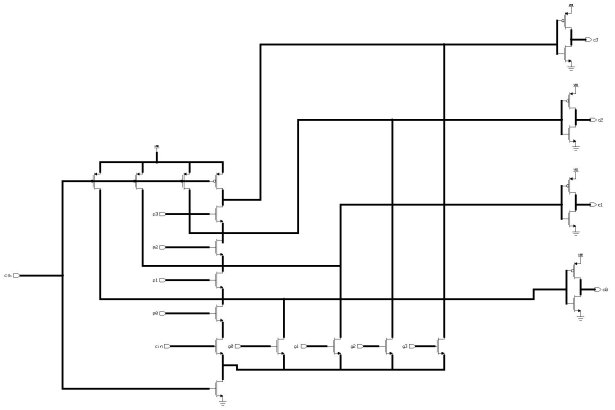

Fig. 6: Carry Chain of Proposed Adder

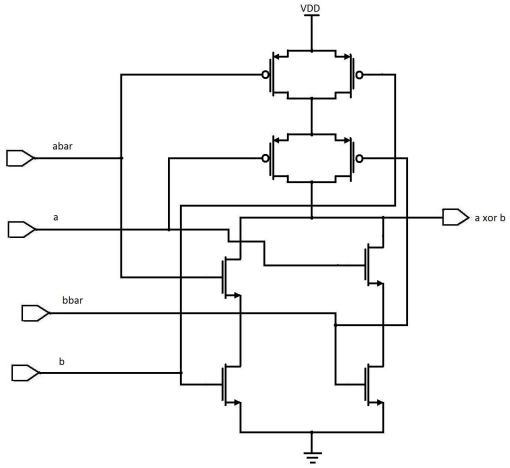

Fig. 5: Conventional XOR

since the change in input signal should gate the transistor that is nearest to the precharged output node.

2) PTL implementation of XOR gate results in the use of less number of transistors, in turn results in less energy consumption for arithmetic functions which contains XOR gates.

The Fig.6 shows the circuit diagram of the manchester carry chain of the proposed adder. It uses a total of 25 transistor where as the conventional manchester carry chain requires 27 transistor for its implementation. The proposed carry chain is based on multiple output domino logic, and the weak pMOS is connected to the ground. The XOR implementation of the proposed adder is shown in Fig.7. It is based on Pass Transistor Logic and hence it uses only 4 transistor.

The block representation of the proposed 32 bit adder was shown in Fig. 8. It is based on the ripple carry adder topology and hence the carry_out of the first 4 bit adder block is fed to the carry_in of the next 4 bit adder block .

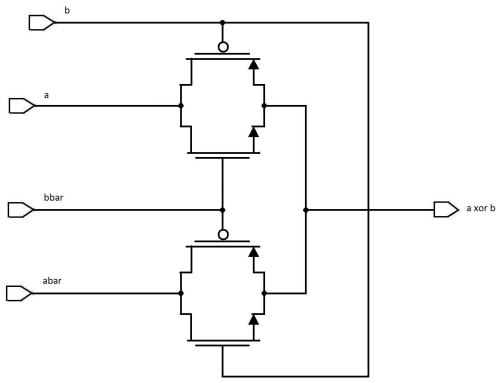

Fig. 7: 4T XOR implementation

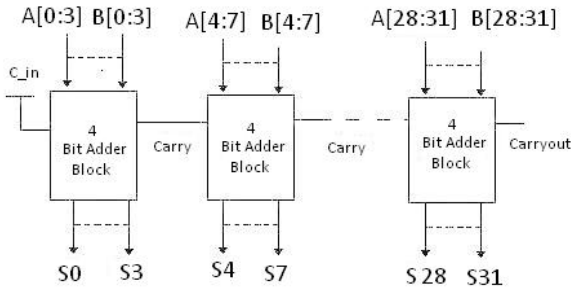

Fig. 8: Block Representation of 32 Bit Adder

V. Experimental Results

The 4 bit block of CMCC (Conventional Manchester Carry Chain) Adder and MMCC (Modified Manchester Carry Chain) was cascaded in ripple carry adder topology. The 32 bit CMCC adder and MMCC adder was implemented by cascading 4 bit block of these adders in ripple carry adder topology. The schematic entry of the 4 bit block was done using Mentor Graphics Design Architect. After that, the 4 bit blocks are cascaded to obtain 32 bit adder. The implemented 32 bit

adder was simulated using Mentor Graphics ELDO. The clock signal and all the input pattern signals have voltage(vhi) of 1.5v, and the t_rise(Rist time) = t_fall(Fall Time) = 100pS. The following parameters are used for simulation. Wpmos = 240nm; Wnmos = 360nm. The results are obtained by giving different combination of input patterns, selected randomly.

A. Area Comparison

The CMCC adder requires 1128 transistors for its implementation whereas the MMCC adder requires only 864. This shows a decrease of 23.4% area. This reduction in area resuls in getting better PDAP(power delay Area product) for MCC adder.

B. Delay Comparison

The delay of 32 bit adders are compared by giving same input patterns to these two adders and the delay for producing the final carry(Carryout in Fig. 8) is measured. The Fig. 10 shows the delay measurements and Table 2 shows the Delay comparision. The simulation results shows that the delay of these two adders are around the same value and the MMCC adder have the least.

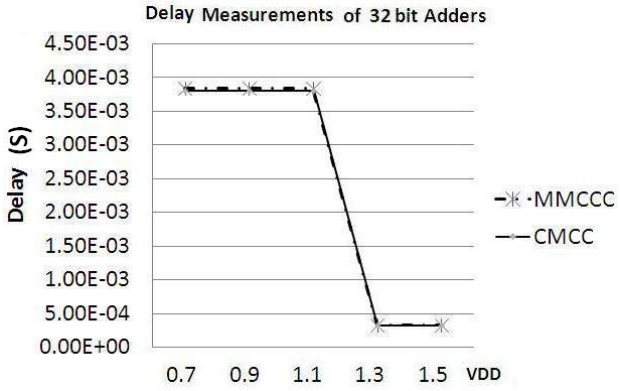

Fig. 9: Delay Measurements of 32 bit Adders

Table 1 Delay Comparison

VDD	CMCC Adder	MMCC Adder	Δ%
1.5V	32.00E-05	31.87E-05	-.40%
1.3V	32.00E-05	31.87E-05	-.40%
1.1V	32.00E-05	31.87E-05	-.40%
.9V	38.30E-05	38.00E-05	-.70%
.7V	38.30E-05	38.00E-05	-.70%

C. Power Comparison

The two 32 bit adders are simulated at different VDD values from .7v to 1.5V and the power is measured. The Fig. 9 shows the power measured using Mentor graphics ELDO. The comparison table of power measurements of CMCC adder and MMCC adder is shown in Table 1. The MMCC adder consumes 14.86% more power compared to that of CMCC adder.

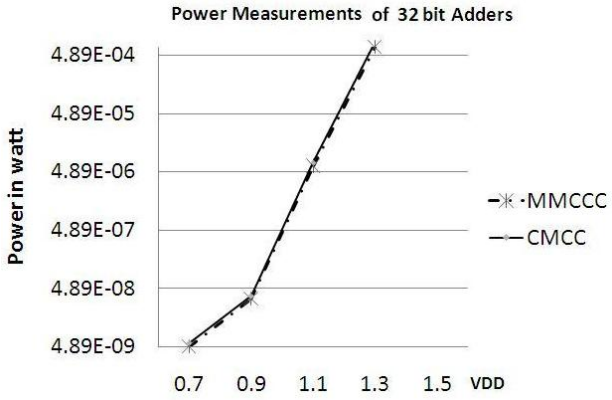

Fig. 10: Power Measurements of 32 bit Adders

Table 2 Power Comparison

VDD	CMCC Adder	MMCC Adder	Δ%
1.5V	48.9E-10	56.17E-10	+14.86%
1.3V	31.65E-09	36.35E-09	+14.84%
1.1V	60.63E-07	69.92E-07	+15.32%
.9V	66.92E-05	77.28E-05	+15.48%
.7V	77.04E-05	89.08E-05	+15.62%

The PDAP of the two adders were calculated and the result was tabulated in Table 3. The PDAP of the MMCC adder get increased by 12.5%. The physical layouts (without IO ports) of the carry chain of CMCC adder and MMCC adder are shown in Fig. 11 and Fig. 12. Mentor Graphics IC Station was used for creating the schematic driven layout by using design view point created in Mentor Graphics Design Architect.

Table 3 PDAP Comparison

Parameter	CMCC Adder	MMCC Adder	Δ%
Power	48.9E-10	56.17E-10	+14.86%
Delay	32.00E-05	31.87E-05	-.40%
Area	1128	864	+23.4%
PDAP	1.76E-09	1.54E-09	+12.5%

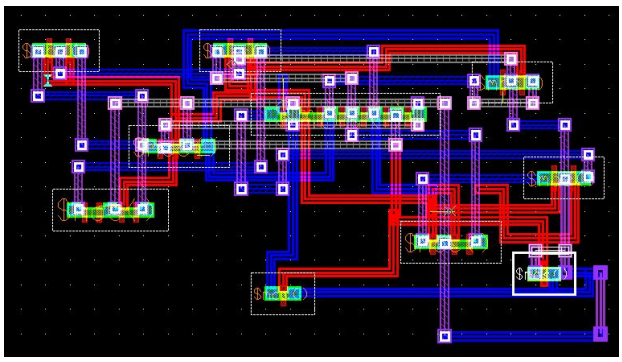

Fig. 11: Layout of carry chain of CMCC Adder

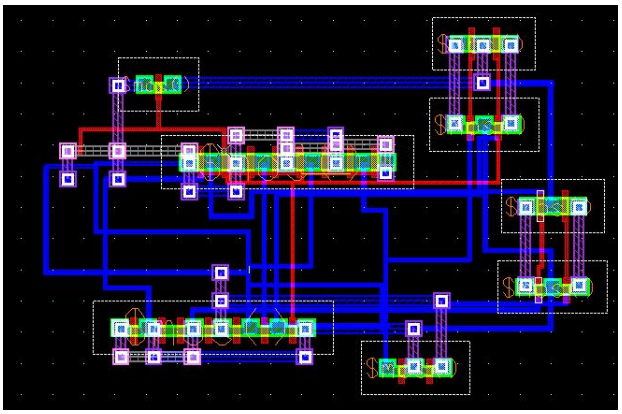

Fig. 12: Layout of carry chain of MMCC Adder

VI. Conclusion

In the proposed design a 32 bit adder is implemented using modified Manchester chain and 4T XOR implementation in ripple carry topology. The proposed design is much more area efficient compared to implementation of 32 bit adder in conventional Manchester chain and XOR design style. The proposed 32 bit adder is shown in Fig.8. The proposed 32 bit adder uses a total number of 864 transistors where as the coventional implementation requires 1128 transistors. Thus the result shows a reduction of 23.4% in size by sacrificing power consumption by a value of 14.86% without affecting the delay. The PDAP get increased by 12.5%. The schematic entry was done using mentor graphics Design architect and simulation was done using Mentor Graphics ELDO. The simulation was done using TSMC 180nm process technology at 1.5v.

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